Manual of compact models for Double-Barrier Magnetic Tunnel Junction (MTJ)

SPINLIB: Model DMTJ

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I. General Introduction

Magnetic tunnel junctions (MTJs) composed of ferromagnetic layers with perpendicular magnetic anisotropy (PMA) are of great interest for achieving high-density non-volatile memory and logic chips owing to its scalability potential together with high thermal stability. Recent progress has demonstrated a capacity for high speed performance and low power consumption through current-induced magnetization switching. In this manual, we present the utilization of a compact model of CoFeB/MgO double-barrier MTJ (DMTJ), a system exhibiting the best tunnel magneto-resistance ratio and switching performance. Furthermore, Combination of double-barrier and synthetic double-free layers can heighten the STT effect and enhance the thermal stability simultaneously. Larger STT switching efficiency, compared with conventional MTJ, can thus be realized. The MTJ key structure consists of $Co_{20}Fe_{60}B_{20}$(1.2)/MgO(0.4)/$Co_{20}Fe_{60}B_{20}$(1.6)/Ta(0.4)/ $Co_{20}Fe_{60}B_{20}$(1.0)/MgO(0.8)/$Co_{20}Fe_{60}B_{20}$(1.2) (numbers are nominal thicknesses in nanometers) (see Fig1(a)). It integrates the physical models of static, dynamic; many experimental parameters are directly included to improve the agreement of simulation with measurements.

The objective of this guide is to provide an easy way to start the simulation of hybrid DMTJ/CMOS circuits.

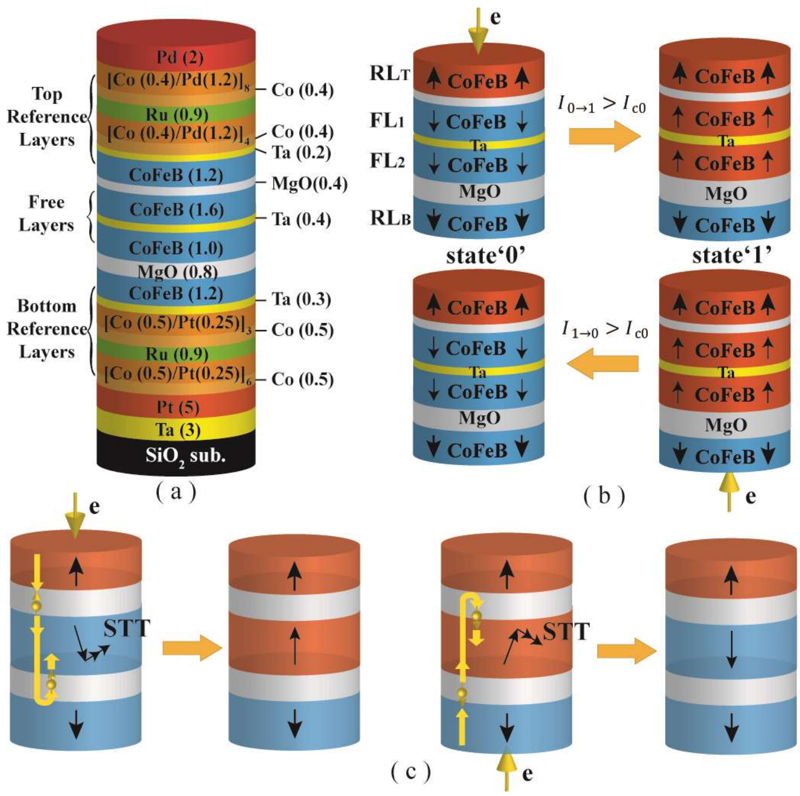


Fig. 1 (a) The structure of Ta/CoFeB/MgO PMA DMTJ with synthetic double free layers, the unit of the thickness of the layers is nm, FL represents free layer, RL represents reference layer. (b) The STT switching mechanism for the DMTJ: '0' and '1' represent the low resistance state and the high resistance state respectively. The state changes from '0' to '1' as the positive direction current $I_{0\to1}>I_{C0}$; and the state will change back as the negative direction current $|I_{1\to0}|>|I_{C0}|$. (c) The diagram of the enhanced STT effect arising from the two tunnel barriers in DMTJ.

Programmed with Verilog-A language
Validated in Cadence 6.1.5 Spectre, CMOS Design Kit 28nm and 40nm.

II. Files Provided

Decompress the compressed file DMTJ model.tar which you have downloaded (Attention: Never rename the model out of Cadence, or a hierarchical problem would occur.).

There are ***three*** files included in the decompressed file:

The first file named **“modelPMAMTJ”** includes a script file of the type of veriloga, which is the source code of this model, and a symbol file (original symbol).

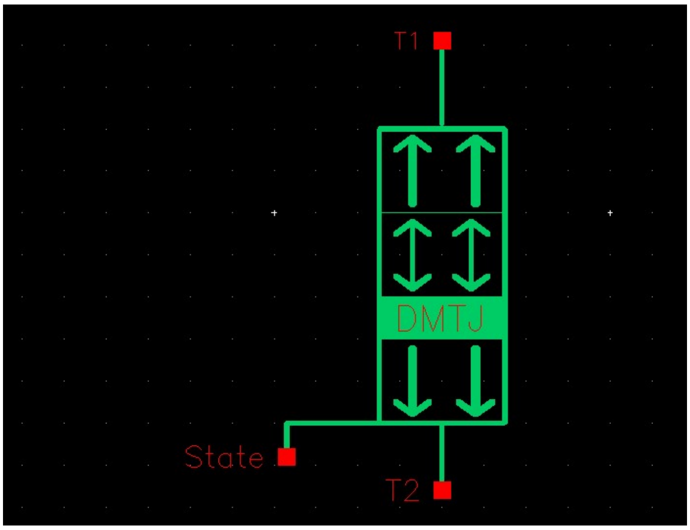


Fig.2 Symbol of the PMAMTJ model

The second file named **“cellPMAMTJ”** includes a package schematic designed with the original symbol and a symbol file of PMAMTJ (formal symbol).
This symbol contains three pins:

A virtual output pin “State” is used to test the state of MTJ. Its output must be one of the two discrete voltage-levels: level ‘0’ indicates the parallel state; level ‘1’ indicates the anti-parallel state.

Another two pins “T1, T2” are the real pins of the junction. These two pins aren’t symmetric: a positive current entering the pin “T1” can make the state change from parallel to anti-parallel.

Another file named “**DC simulation**” is a simple test simulation case using this model in order to demonstrate how it works. The schematic of the test simulation is shown in Fig. 3. We apply a simple voltage pulse as input to generate a bi-directional current which can switch the state of DMTJ from parallel to anti-parallel or from anti-parallel to parallel. By monitoring the voltage-level of the pin “State” and the current values passing through the DMTJ, we can validate this compact model. The results of DC and transient simulations are presented in Fig.4 and Fig.5.

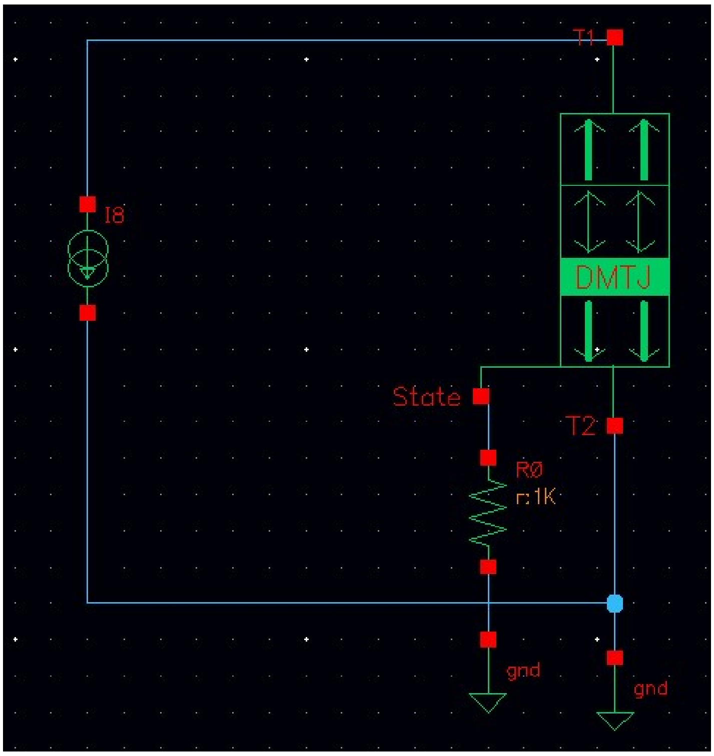


Fig.3 Schematic of the test simulation

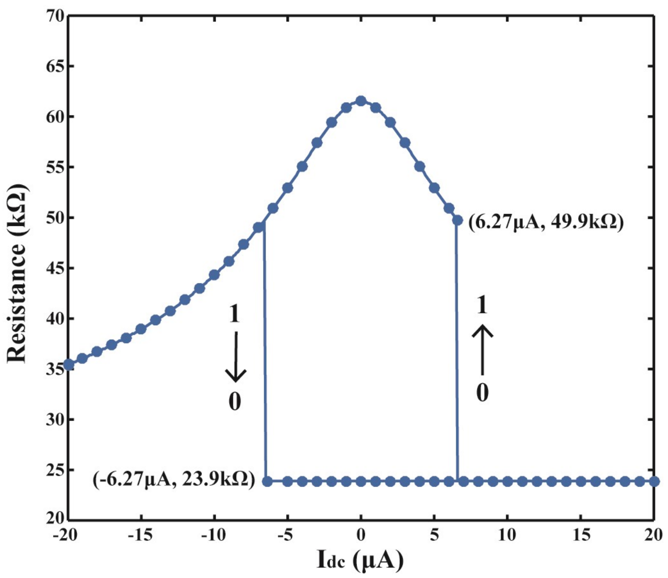


Fig.4 DC simulation of the DMTJ model

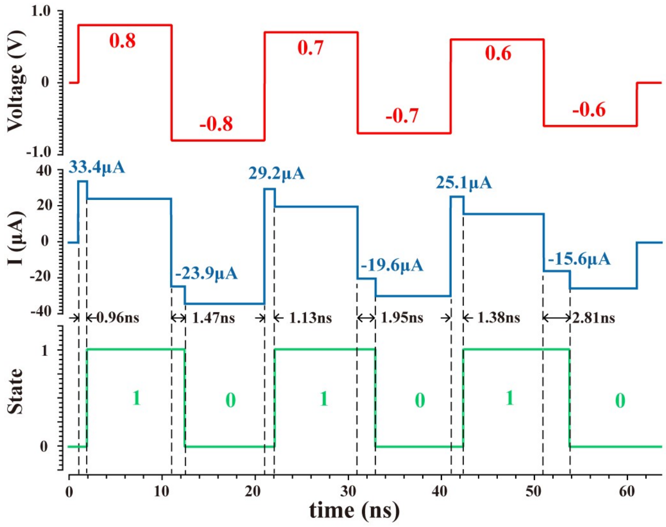


Fig.5 Transient simulation result of DMTJ model

III. Parameters

III.A Component Description Format (CDF)

In order to describe the parameters and the attributes of the parameters of individual component and libraries of component, we use the Component Description Format (CDF). It facilitates the application independent on cellviews, and provides a Graphical User Interface (the Edit Component CDF form) for entering and editing component information.

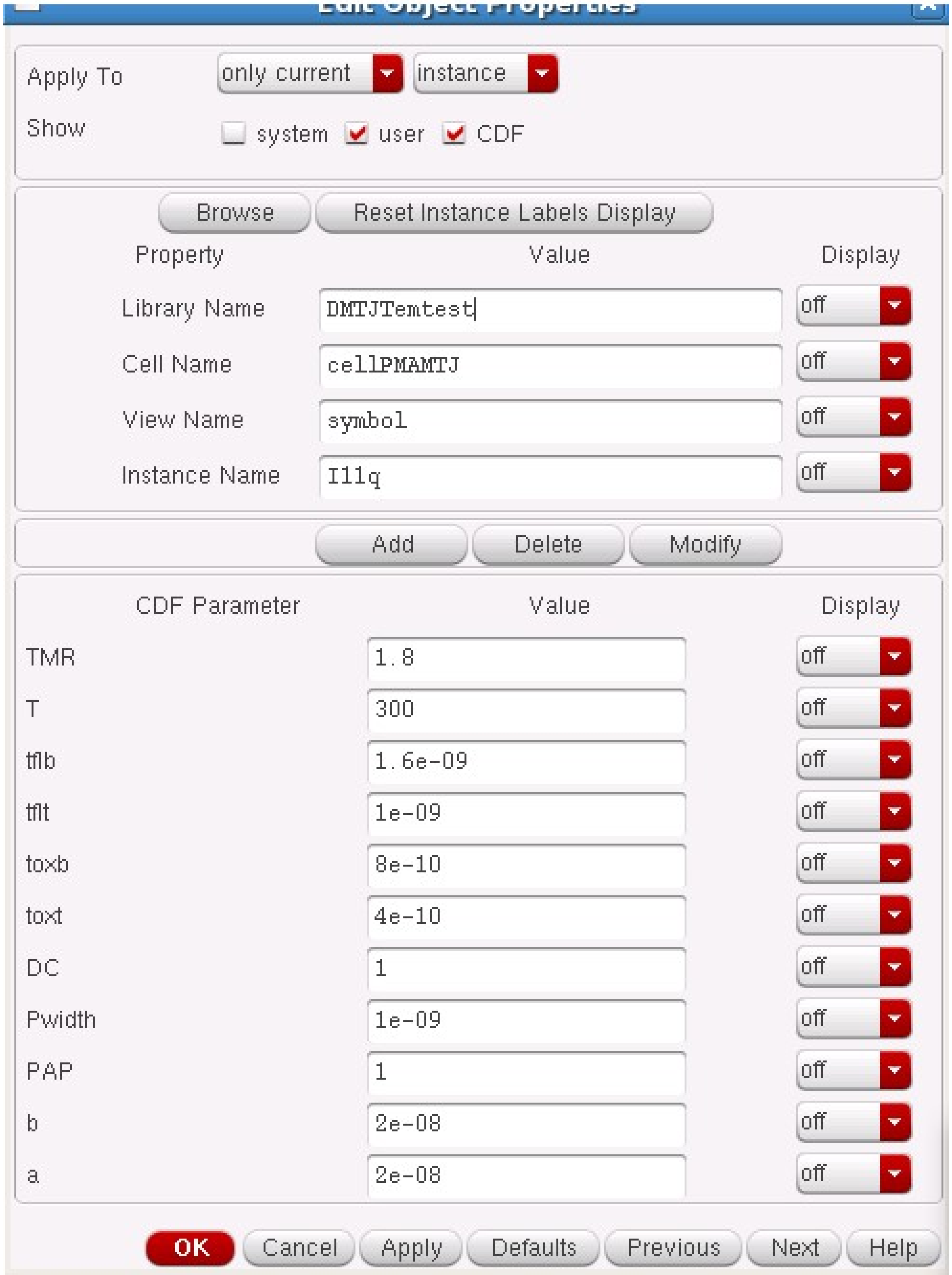


Fig.6 Modify the CDF parameters

Thanks to its favorable features, we use CDF to define the initial state of PMA MTJ. By entering “0” or “1” in the column “PAP” in category “Property”, we can modify the initial state to parallel or antiparallel (see Fig.6). Furthermore, using CDF tools we can modify multi MTJs’ states individually, which facilitates implementation of more complex hybrid CMOS/MTJ circuits.

If you need to define other parameters for this library, you can click Tools -> CDF -> Edit, enter “PMAMTJ” as the Library Name and “cell_PMAMTJ” as the Cell Name. Select “Base” as the CDF Type. Then click “Add” under Component Parameters. (see Fig.7)

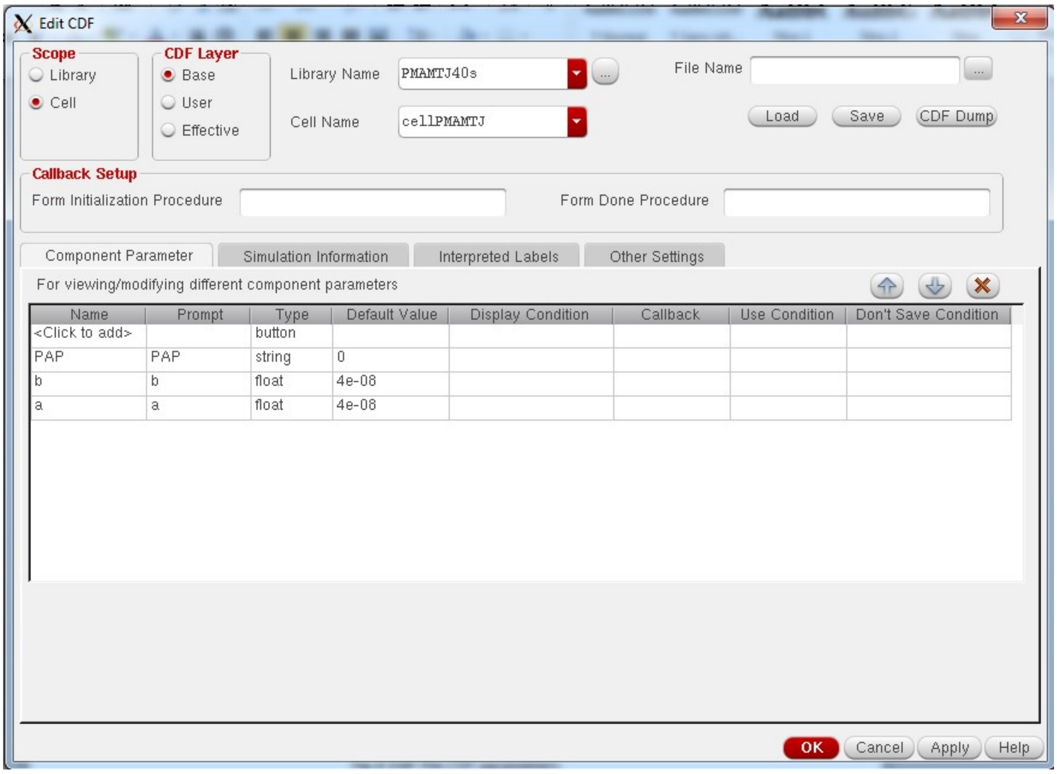


Fig.7 Edit the CDF parameters

Fill out the form as shown in Fig.7. You need to select the type of the parameter and enter the name and defValue of the parameter. Then click “OK”.

III.B Technology Parameters

TABLE 1

PARAMETERS AND THEIR DEFAULT VALUES IN DMTJ PHYSICAL MODELS

Parameter	Description	Default Value
V_{half}	Reference voltage for bias voltage TMR model	0.5V
K_B	Bulk anisotropy of free layer	1.8×10^{5} J/m^3
K_I	Interface anisotropy of free layer	1.3×10^{-3} J/m^2
M_S	Saturation magnetization	1.58 T
As	Exchange stiffness constant	19 pJ/m
P	Spin polarization percentage	0.71
e	Elementary charge	1.6×10^{-19} C
γ	Gyromagnetic ratio	1.76×10^{11}rad/T
μ_B	Bohr magneton	9.274×10^{-24} J/T
α	Damping constant	0.004
kB	Boltzmann constant	1.38×10^{-23} J/K
T	Kelvin temperature	300 K

These technology parameters depend mainly on the material composition of the MTJ nanopillar and it is recommended to keep their default value.

III.C Device Parameters

Parameter	Description	Default value (Range)
t_{OXT}	Top barrier thickness	0.8 nm
t_{OXB}	Bottom barrier thickness	0.4 nm
t_{FLT}	Top free layer thickness	1.6 nm
t_{FLB}	Bottom free layer thickness	1.0 nm
a	Length of surface long axis	20 nm
b	Width of surface short axis	20 nm
TMR	TMR(0) with Zero Volt Bias Voltage	180% (50%-600%)

These device parameters depend mainly on the process and mask design and the designers can change them to adapt their requirements.

The default shape of MTJ nanopillar surface is circular (a=b), but we can use also ellipse for specific simulation purposes.

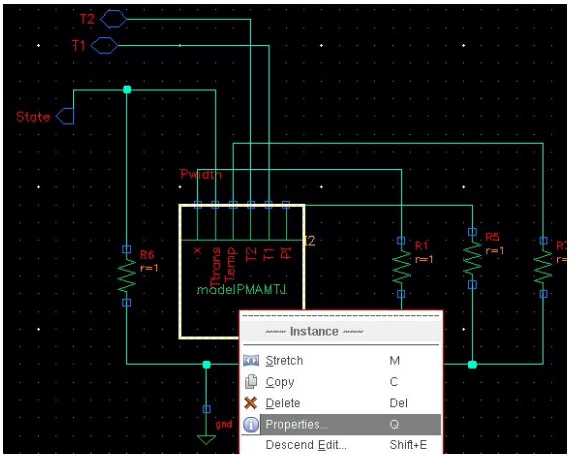
IV. Before simulation

1. When you launch ADE L for a new simulation under Cadence, check if you have added “veriloga hdl” in the “switch view list” from “Setup”.
2. Check if the Temperature setting is “300”(300K).
3. Check if there are user parameters or variables which are not aligned with appropriate values.

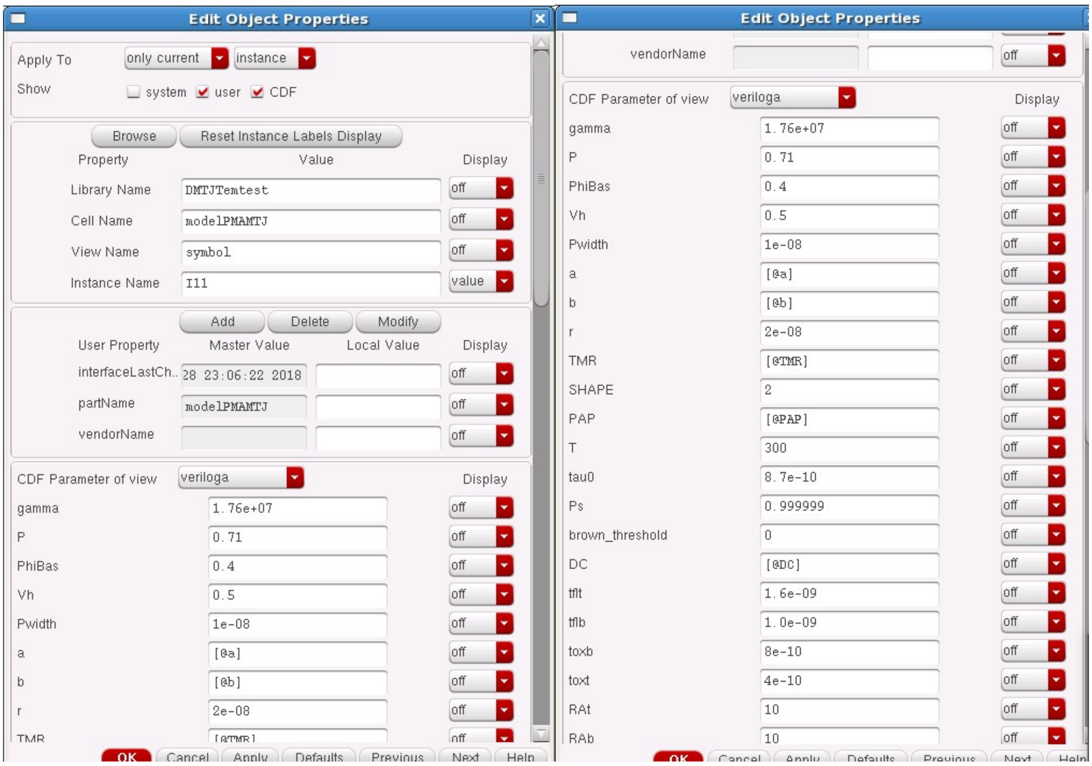
Start the simulation after having four “yes” for the questions above.
If the parameter values of your MTJ is very different from ours, you can modify the parameters as follows:

(1) Open the file cellPMAMTJ->schematic

(2) Click modelPMAMTJ->properties



(3) Then configure the parameters as you want:



Reference

[1] G. D. Wang, Y. Zhang, J. K. Wang, Z. Z. Zhang, K. Zhang, Z. Y. Zheng, J. O. Klein, D. Ravelosona, Y. G. Zhang and W. S Zhao, "Compact Modeling of Perpendicular-Magnetic-Anisotropy Double-Barrier Magnetic Tunnel Junction with Enhanced Thermal Stability Recording Structure," Early Access. DOI: 10.1109/TED.2019.2906932

This paper describes the technical details and performance analysis of DMTJ model, 1-bit DMTJ-MFA, as a logic-in-memory circuit example, has been designed to validate the functionality of our proposed model. 1-bit DMTJ-MFA, as a logic-in-memory circuit example, has been designed to validate the functionality of our proposed model.

Welcome to use our model! Thank you!

If you have any questions, contact with gdwangbuaa@qq.com.